



INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)			Complete if Known		
			Application Number	10/673,211	
			Filing Date	September 30, 2003	
			First Named Inventor	Xavier Montagne	
			Art Unit	2858	
			Examiner Name	TBA	
Sheet	1	of	1	Attorney Docket Number	003921.00136

U.S. PATENT DOCUMENTS						
Examiner Initials *	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
		Number - Kind Code ² (if known)				
DG		US- 6,473,726	10-29-2002	Reblewski		
DG		US-6,265,894	07-24-2001	Reblewski et al.		
DG		US- 6,184,707	02-08-2001	Norman et al.		
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DG		US- 5,038,473	07-30-1991	Butts et al.		
FOREIGN PATENT DOCUMENTS						
Examiner Initials *	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ³
		Country Code ⁴ - Number ⁴ - Kind Code ⁵ (if known)				
DG		WO 94/06210	03-17-1994	Prabhakar Goel		
DG		EP 0 651 343	05-03-95	Quickturn Systems, Inc.		
NON PATENT LITERATURE DOCUMENTS						
Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				T ²
DG		CHARLES CLOS, "A Study of Non-Blocking Switching Networks", The Bell System Technical Journal, March 1953, pages 408-424				
DG		WERNER ERHARD et al., "First Steps towards a Reconfigurable Asynchronous System", Friedrich-Schiller University Jena, Department of Computer Science, IEEE International Workshop on Rapid System Prototyping, June 1999, pages 28-31				
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DG		GREG SNIDER, "The Teramac Compiler", Hewlett-Packard, 1996, pages 1-51				
DG		Xilinx, "Programmable Gate Array Design Handbook", First Edition, 1988, pages i-A10				
DG		JONATHAN BABB, et al., "Logic Emulation with Virtual Wires", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, June 1997, pages 1-20				
Examiner Signature	<i>[Signature]</i>			Date Considered	2/22/2006	

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